FIGURE 1

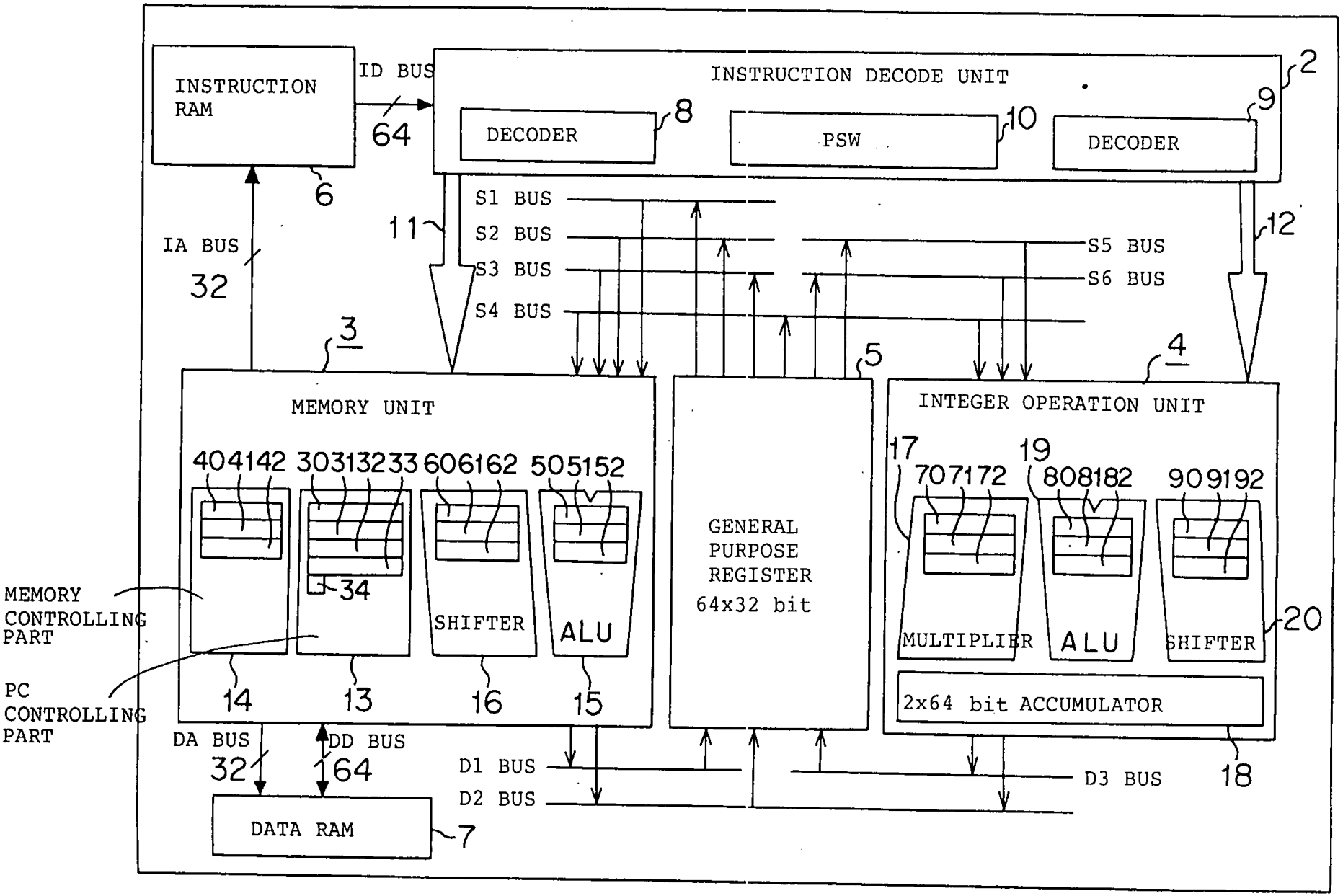
INSTRUCTION RAM
ID BUS
64
6
INSTRUCTION DECODE UNIT
2
DECODER
8
PSW
10
DECODER
9
11
12
S1 BUS
S2 BUS
S3 BUS
S4 BUS
S5 BUS
S6 BUS
IA BUS
32
3
5
4
MEMORY UNIT
INTEGER OPERATION UNIT
404142
30313233
606162
505152
17
19
707172
808182
909192
GENERAL PURPOSE REGISTER
64x32 bit
34
SHIFTER
ALU
MULTIPLIER
ALU
SHIFTER
20
MEMORY CONTROLLING PART
PC CONTROLLING PART
14
13
16
15
2x64 bit ACCUMULATOR
DA BUS
32
DD BUS
64
D1 BUS
D2 BUS
D3 BUS
18
DATA RAM
7

FIGURE 2 (a)

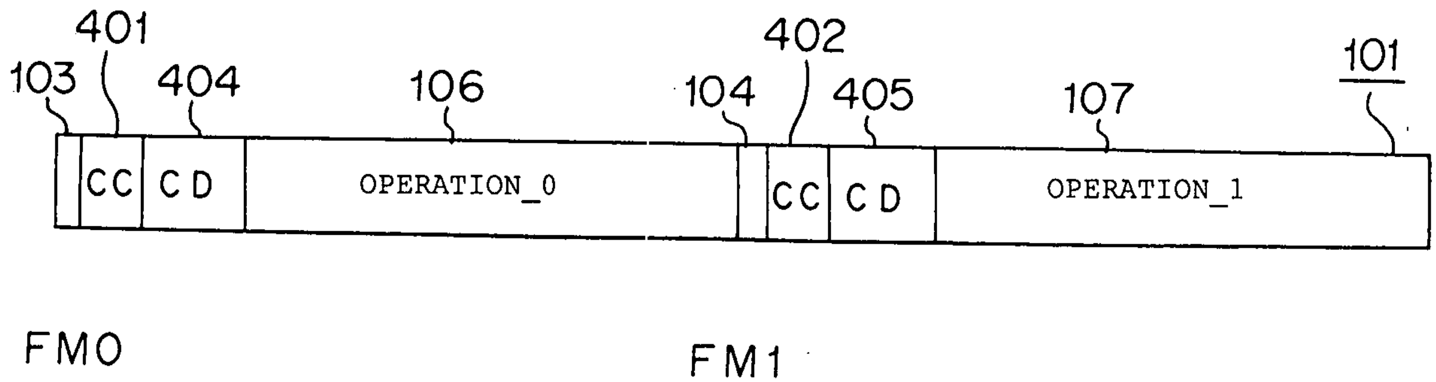

FIGURE 2 (b)

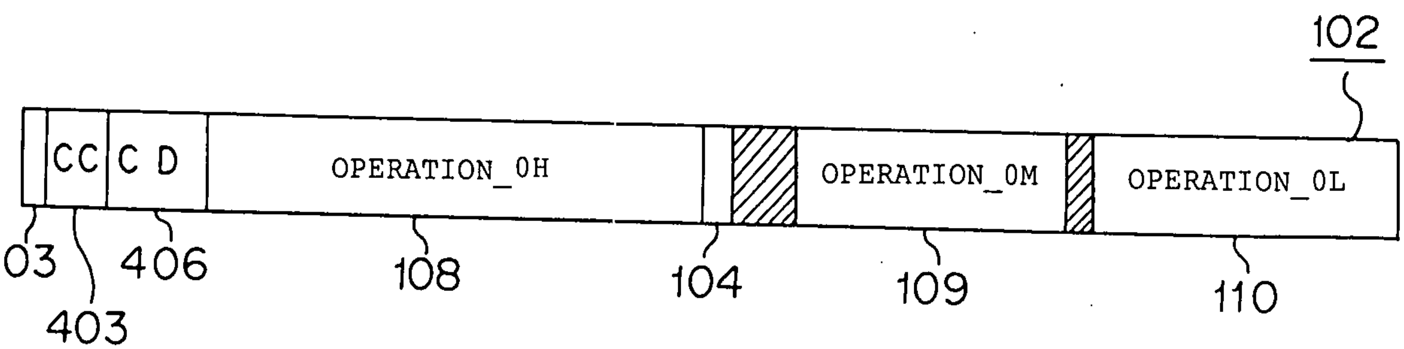

FIGURE 3 (a)

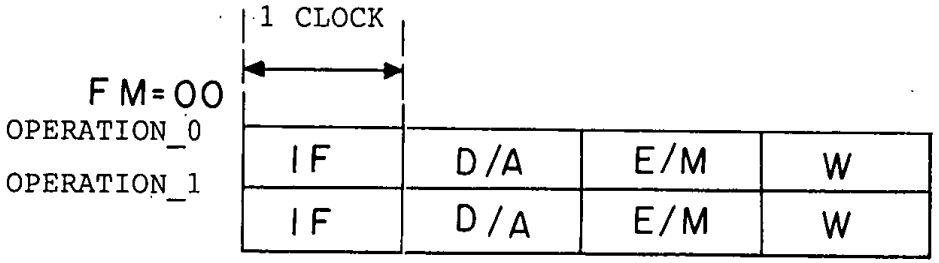

FIGURE 3 (b)

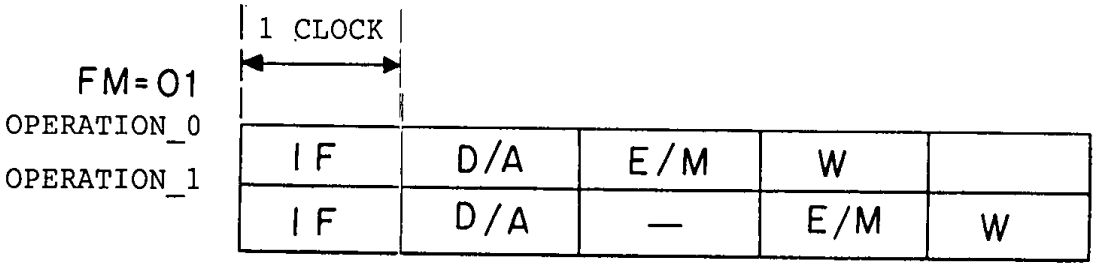

FIGURE 3 (c)

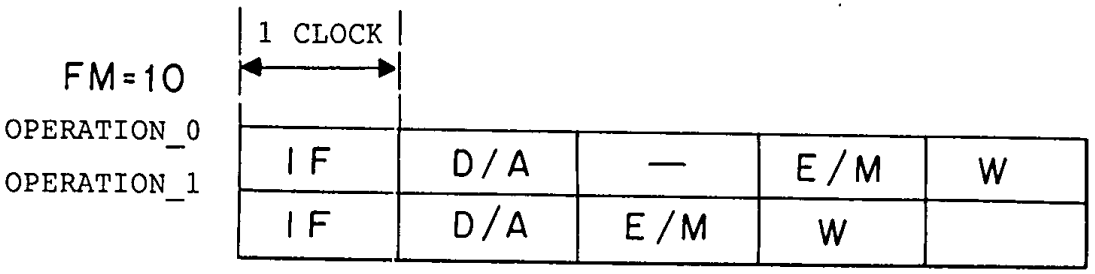

FIGURE 4

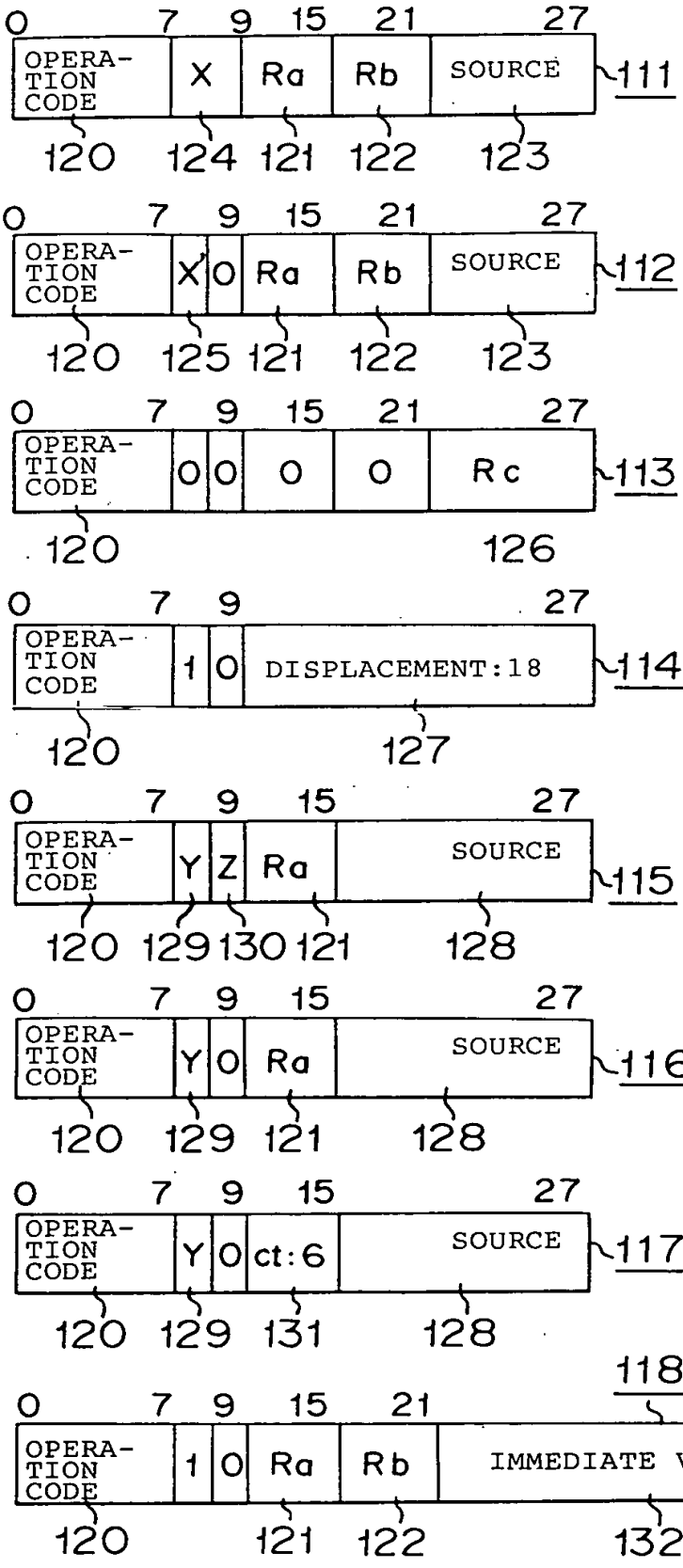
0 7 9 15 21 27
OPERA-TION CODE
X
Ra
Rb
SOURCE
111
120 124 121 122 123
(123)
X=00=>SOURCE=Rc
X=01=>SOURCE=Rc;Rb++
X=11=>SOURCE=Rc;Rb--
X=1-=>SOURCE=IMMEDIATE VALUE:6
0 7 9 15 21 27
OPERA-TION CODE
X'
0
Ra
Rb
SOURCE
112
120 125 121 122 123
(123)
X'=0=>SOURCE=Rc
X'=1=>SOURCE=IMMEDIATE VALUE:6
0 7 9 15 21 27
OPERA-TION CODE
0 0
0
0
Rc
113
120 126
0 7 9 27
OPERA-TION CODE
1 0
DISPLACEMENT:18
114
120 127
(129)
Y=0=>SOURCE=Rc
Y=1=>SOURCE=IMMEDIATE VALUE:12
Z=0=>FOR TESTING ZERO
Z=1=>FOR TESTING OTHER THAN ZERO
0 7 9 15 27
OPERA-TION CODE
Y
Z
Ra
SOURCE
115
120 129 130 121 128
0 7 9 15 27
OPERA-TION CODE
Y 0
Ra
SOURCE
116
120 129 121 128
0 7 9 15 27
OPERA-TION CODE
Y 0
ct:6
SOURCE
117
120 129 131 128
118
0 7 9 15 21 53
OPERA-TION CODE
1 0
Ra
Rb
IMMEDIATE VALUE: 32
120 121 122 132

FIGURE 5 (a)

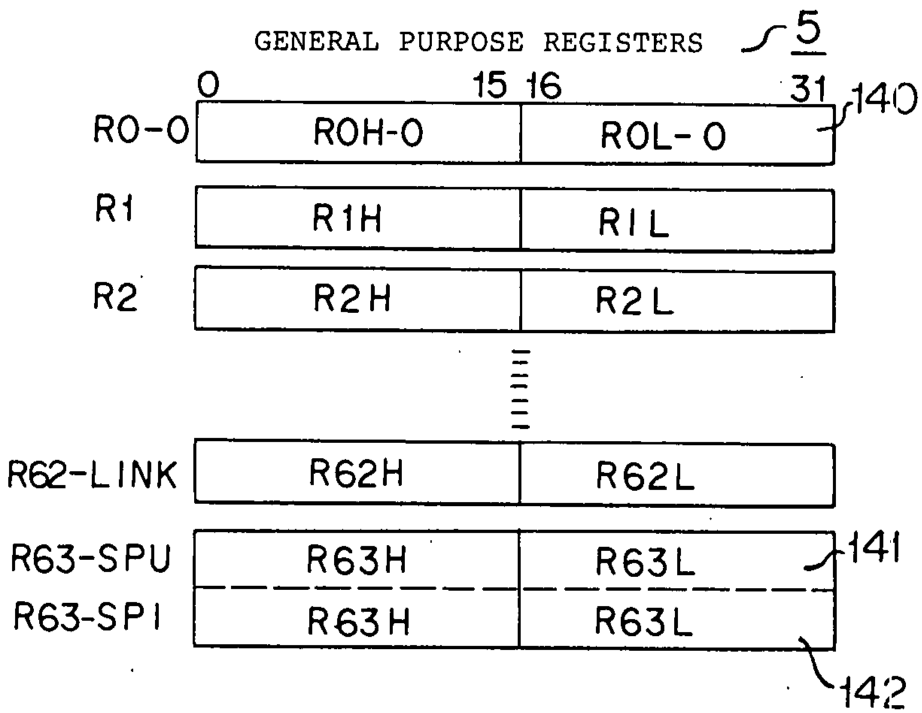

FIGURE 5 (b)

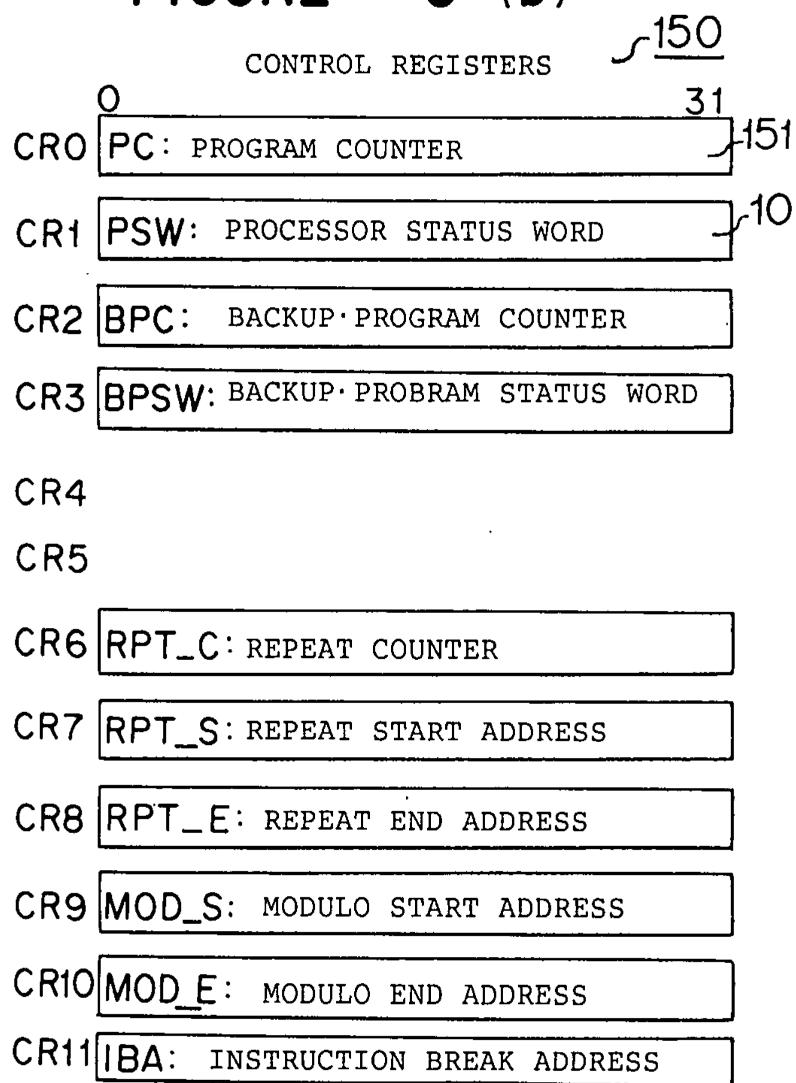
CONTROL REGISTERS
150
0
31
CR0
PC: PROGRAM COUNTER
151
CR1
PSW: PROCESSOR STATUS WORD
10
CR2
BPC: BACKUP·PROGRAM COUNTER
CR3
BPSW: BACKUP·PROBRAM STATUS WORD
CR4
CR5
CR6
RPT_C: REPEAT COUNTER
CR7
RPT_S: REPEAT START ADDRESS
CR8
RPT_E: REPEAT END ADDRESS
CR9
MOD_S: MODULO START ADDRESS
CR10
MOD_E: MODULO END ADDRESS
CR11
IBA: INSTRUCTION BREAK ADDRESS

FIGURE 5 (c)

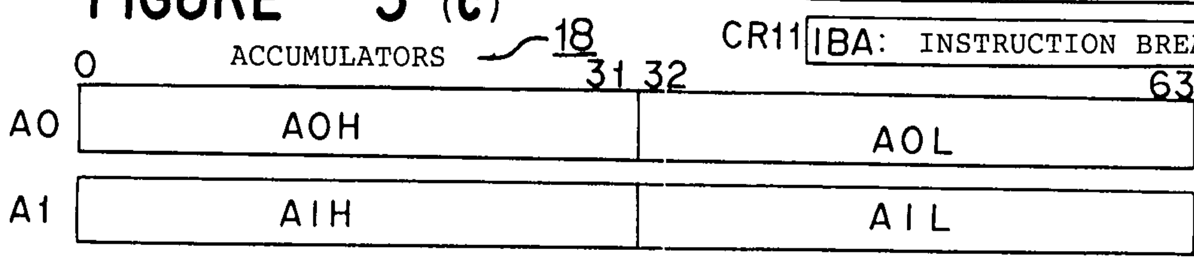

FIGURE 6

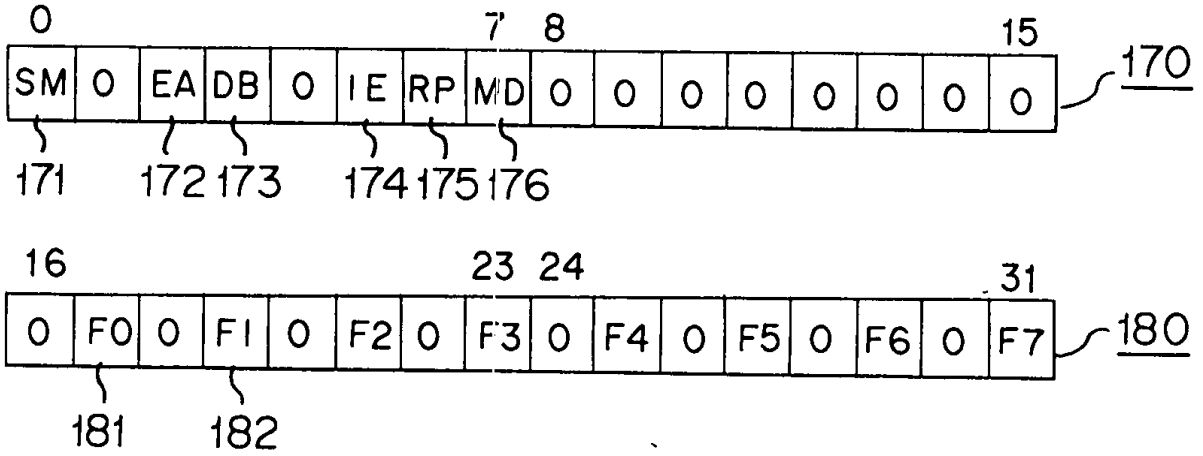

FIGURE 7

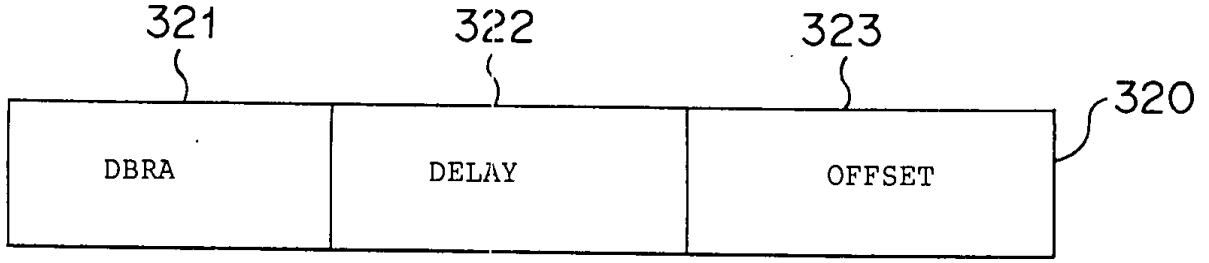

FIGURE 8

INSTRUCTION ADDRESS		OPERATION_0	OPERATION_1
H'1000		I01 (BRA FOF #H'20 loop)	I02:
H'1008	loop:	I11	I12:
H'1010		I21 (ADD R2,R2,R3)	I22:
H'1018		I31 (CMPEO R2,R4,F0)	I32:
H'1020	end:	I41	I42:
H'1028		I51	I52:
H'1030		I61	I62:

FIGURE 9

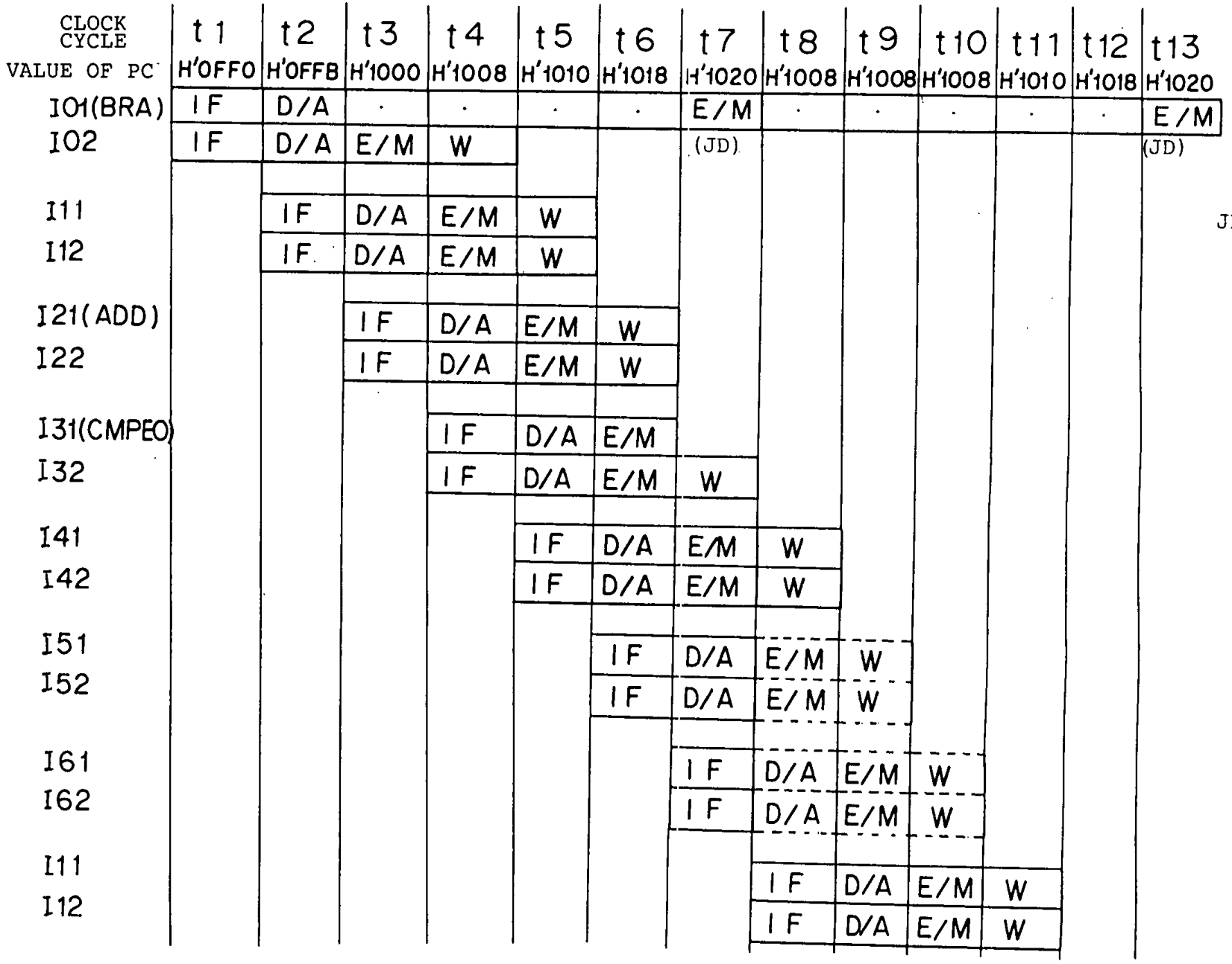
CLOCK CYCLE
VALUE OF PC
t1 H'0FF0
t2 H'0FFB
t3 H'1000
t4 H'1008
t5 H'1010
t6 H'1018
t7 H'1020
t8 H'1008
t9 H'1008
t10 H'1008
t11 H'1010
t12 H'1018
t13 H'1020
I01(BRA) IF D/A . . . . E/M . . . . . E/M
I02 IF D/A E/M W (JD) (JD)
I11 IF D/A E/M W
I12 IF D/A E/M W
I21(ADD) IF D/A E/M W
I22 IF D/A E/M W
I31(CMPEQ) IF D/A E/M
I32 IF D/A E/M W
I41 IF D/A E/M W
I42 IF D/A E/M W
I51 IF D/A E/M W
I52 IF D/A E/M W
I61 IF D/A E/M W
I62 IF D/A E/M W
I11 IF D/A E/M W
I12 IF D/A E/M W
JD: JUDGING CONDITION

FIGURE 10

INSTRUCTION ADDRESS	OPERATION_0	OPERATION_1
H' 1000	I01 (DJMP FOT #H'18 #H'28 R5)	I02:
H' 1008	I11 (ADD R1, R1, R2)	I12:
H' 1010	I21 (CMPEQ R1, R3, F0)	I22:
H' 1018	I31 (ADD R5, R5, R6)	I32:
H' 1020	I41	I42:
H' 1028	I51	I52:
H' 1030	I61	I62:
H' 1038	I71	I72:

FIGURE 11

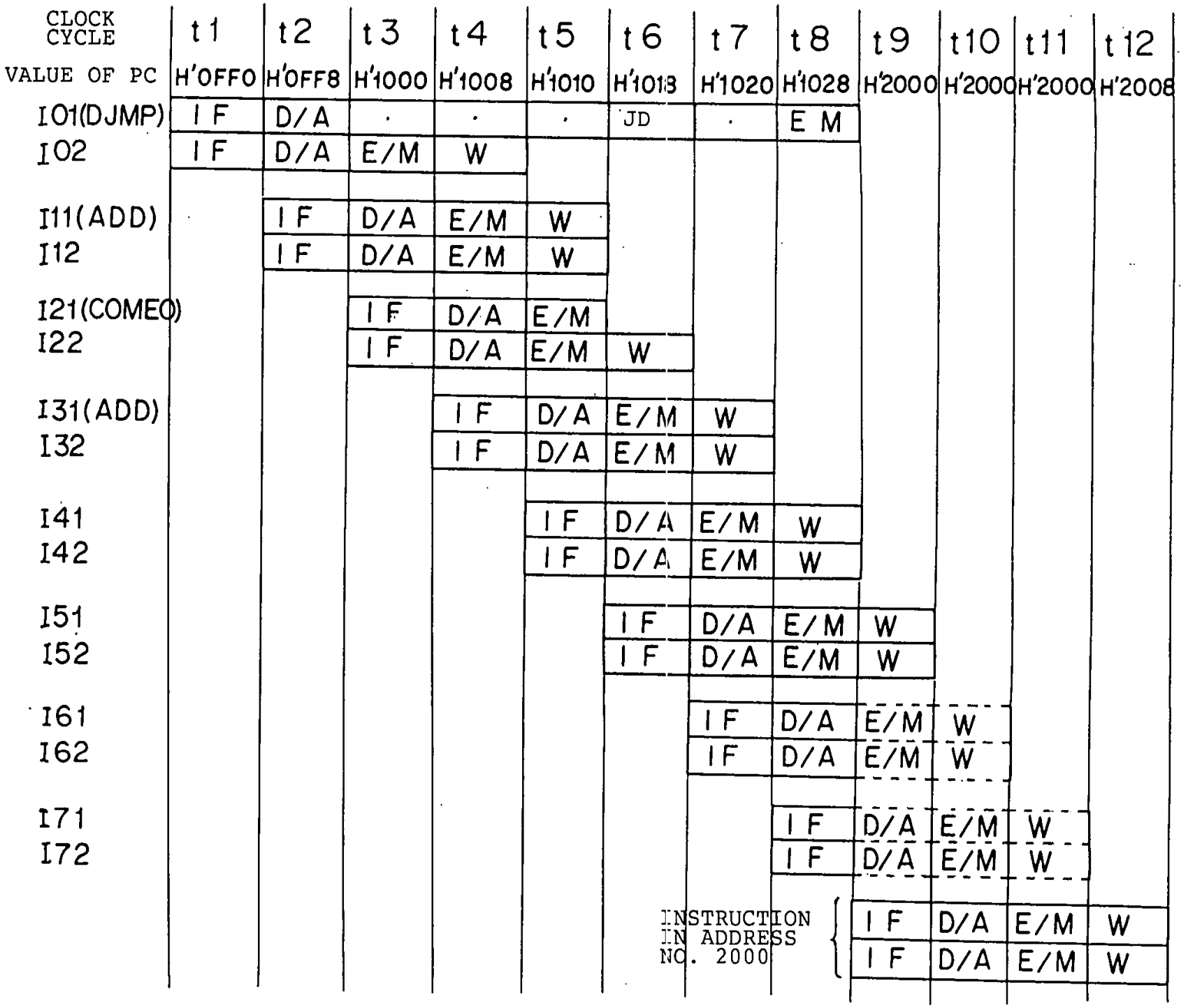
CLOCK CYCLE
t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12
VALUE OF PC
H'0FF0 H'0FF8 H'1000 H'1008 H'1010 H'1018 H'1020 H'1028 H'2000 H'2000 H'2000 H'2008
I01(DJMP) I F D/A · · · JD · E M
I02 I F D/A E/M W
I11(ADD) I F D/A E/M W
I12 I F D/A E/M W
I21(COMEO) I F D/A E/M
I22 I F D/A E/M W
I31(ADD) I F D/A E/M W
I32 I F D/A E/M W
I41 I F D/A E/M W
I42 I F D/A E/M W
I51 I F D/A E/M W
I52 I F D/A E/M W
I61 I F D/A E/M W
I62 I F D/A E/M W
I71 I F D/A E/M W
I72 I F D/A E/M W
INSTRUCTION IN ADDRESS NO. 2000
I F D/A E/M W
I F D/A E/M W
JD: JUDGING CONDITION

FIGURE 12